IN THE CLAIMS

Please amend the claims as follows. This listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently Amended) A system of multiplexed data lines in a DRAM integrated circuit, comprising:

(a) a switching circuit having a first switching state and a second switching state;

(b) a first data path associated with a first memory portion of the DRAM integrated circuit, the first data path comprising a first plurality of master data lines for the first memory portion of the DRAM integrated circuit;

(c) a second data path associated with a second memory portion of the DRAM integrated circuit, the second data path comprising a second plurality of master data lines for the second memory portion of the DRAM integrated circuit; ~~and~~

(d) a plurality of read-write data lines of the DRAM integrated circuit, wherein the first data path is in communication with the plurality of read-write data lines when the switching circuit is in the first ~~fist~~ switching state, and wherein the second data path is in communication with the plurality of read-write data lines when the switching circuit is in the second switching state;

(e) a first plurality of transmission gates between the first data path and the plurality of read-write data lines, wherein the first plurality of transmission gates conduct in the first switching state and do not conduct in the second switching state; and

(f) a second plurality of transmission gates between the second data path and the plurality of read-write lines, wherein the second plurality of transmission gates conduct in the second switching state and do not conduct in the first switching state.

2. (Cancelled).

3. (Currently Amended) The system of Claim 1 [[2]], wherein the first plurality of transmission gates conduct and the second plurality of transmission gates do not conduct in response to an enable signal.

4. (Original) The system of Claim 3, wherein the first plurality of transmission gates do not conduct and the second plurality of gates conduct in response to an inverse of the enable signal.

5. (Cancelled).

6. (Original) The system of Claim 1 further comprising:

(e) another plurality of read-write data lines of the DRAM integrated circuit, wherein the other plurality of read-write data lines is in communication with the second data path when the switching circuit is in the first switching state, and wherein the other plurality of read-write data lines is in communication with the first data path when the switching circuit is in the second switching state.

7. (Original) The system of Claim 6, wherein the switching circuit further comprises:

(a3) a third plurality of transmission gates between the second data path and the other plurality of read-write data lines, wherein the third plurality of transmission gates conduct in the first switching state and do not conduct in the second switching state; and

(a4) a fourth plurality of transmission gates between the first data path and the other plurality of read-write data lines, wherein the fourth plurality of transmission gates conduct in the second switching state and do no conduct in the first switching state.

8. (Previously Presented) A system of multiplexed data lines in a DRAM integrated circuit, comprising:

(a) a switching circuit having a first switching state and a second switching state;

(b) a first data path associated with a first memory portion of the DRAM integrated circuit;

(c) a second data path associated with a second memory portion of the DRAM integrated circuit;

(d) a plurality of read-write data lines of the DRAM integrated circuit, wherein the first data path is in communication with the plurality of read-write data lines when the switching circuit is in the fist switching state, and wherein the second data path is in communication with the plurality of read-write data lines when the switching circuit is in the second switching state; and

(e) another plurality of read-write data lines of the DRAM integrated circuit, wherein the other plurality of read-write data lines is in communication with the second data path when the switching circuit is in the first switching state, and wherein the other plurality of read-write data lines is in communication with the first data path when the switching circuit is in the second switching state.

9. (Previously Presented) The system of Claim 8, wherein the switching circuit comprises:

(a1) a first plurality of transmission gates between the first data path and the plurality of read-write data lines, wherein the first plurality of transmission gates conduct in the first switching state and do not conduct in the second switching state; and

(a2) a second plurality of transmission gates between the second data path and the plurality of read-write lines, wherein the second plurality of transmission gates conduct in the second switching state and do not conduct in the first switching state.

10. (Previously Presented) The system of Claim 9, wherein the first plurality of transmission gates conduct and the second plurality of transmission gates do not conduct in response to an enable signal.

11. (Previously Presented) The system of Claim 10, wherein the first plurality of transmission gates do not conduct and the second plurality of gates conduct in response to an inverse of the enable signal.

12. (Previously Presented) The system of claim 8, wherein (b) and (c) comprise:

(b1) a first plurality of master data lines for the first memory portion of the DRAM integrated circuit; and

(c1) a second plurality of master data lines for the second memory portion of the DRAM integrated circuit.

13. (Previously Presented) The system of Claim 8, wherein the switching circuit further comprises:

(a3) a third plurality of transmission gates between the second data path and the other plurality of read-write data lines, wherein the third plurality of transmission gates conduct in the first switching state and do not conduct in the second switching state; and

(a4) a fourth plurality of transmission gates between the first data path and the other plurality of read-write data lines, wherein the fourth plurality of transmission gates conduct in the second switching state and do no conduct in the first switching state.